REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated February 22, 2005 (U.S. Patent Office Paper No. 0205). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, Claims 1 through 12 are pending in this application. New Claims 8 through 12 are added, and Claims 1, 5, 6 and 7 are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention.

Prior Art Rejections

Claims 1 through 3 and 5 through 7 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,384,462 to Pauchard et al., hereinafter the Pauchard '462 patent, in view of U.S. Patent No. 6,794,631 to Clark, hereinafter the Clark '631 patent. This rejection is respectfully traversed.

Claim 4 was rejected under 35 U.S.C. § 103(a) over the Pauchard '462 patent modified by the Clark '631 patent, as applied to Claim 1, and further in view of U.S. Patent No. 5,650,635 to Razeghi et al., hereinafter the Razeghi '635 patent. This rejection is respectfully traversed.

It is respectfully submitted that the Clark '631 patent, the Pauchard '462 patent and the Razeghi '635 patent do not disclose:

an avalanche photodiode including a semiconductor interface layer having a wider band-gap than that of the absorption layer is formed between the multiplication layer and the absorption layer, the semiconductor interface layer being securely fused with the multiplication layer, as respectively recited in independent Claims 1, 6 and 7; and

a method of manufacturing an avalanche photodiode, including the steps of: forming a silicon multiplication layer on a silicon substrate; forming, on a substrate, an absorption layer composed of a compound semiconductor and a semiconductor interface layer having a wider band-gap than that of the absorption layer; and fusing the silicon multiplication layer and the semiconductor interface layer, as respectively recited in new Claim 8.

In contrast, conventionally, in the case of directly fusing the silicon multiplication layer and the absorption layer, an impurity enters the absorption layer. On the other hand, the absorption layer is of an easily light absorbed material, which causes a characteristic to make the band-gap narrow. In the other case where the impurity does not enter to the layer or any layers, the band smoothly inclines with an electric field applied. However, in the case where the electric field is applied to the absorption layer with the impurity entered, the band of a portion to which the impurity is entered is largely bent, powerfully applying the electric field to the portion. In the case where the band-gap is narrow such as the absorption layer, a tunnel current (idling current) flows easily due to the narrow band-gap, which can adversely affect the device characteristic.

In contrast, the present invention provides an avalanche photodiode, including a semiconductor interface layer having a wider band-gap width than that of absorption layer, with the interface layer being securely fused with the multiplication layer, and provides a method of manufacturing an avalanche photodiode including fusing the silicon multiplication layer and the semiconductor interface layer. However, when the impurity enters into the interface layer, the tunnel current hardly flows due to the large band-gap even though the band is largely bent in comparison with the narrow band-gap of the absorption layer.

Also, it is respectfully noted that the multiplication layer generally has a wider band-gap than that of the absorption layer in comparison therewith, whereby the affect of the entering of the impurity typically can be neglected.

It is respectfully submitted that the Pauchard '462 patent in view of the Clark '631 Patent does not disclose or teach a semiconductor interface layer being securely fused with a multiplication layer, as respectively recited in Claims 1, 6 and 7. Further, the Pauchard '462 patent in view of the Clark '631 Patent does not disclose or teach fusing a silicon multiplication layer and a semiconductor interface layer, as respectively recited in new Claim 8.

As to the Pauchard '462 patent, the Office Action notes that the Pauchard '462 patent does not disclose an interface layer between the multiplication layer 14 and the absorption layer 11 (U.S. Patent Office Paper No. 0205, page 2).

While the Pauchard '462 Patent discloses an absorption layer 11 fused to silicon wafer 13 (Col. 4, lines 41-43), the Pauchard '462 patent does not teach or suggest an interface layer between the multiplication layer 14 and the absorption layer 11 (U.S. Patent Office Paper No. 0205, page 2). Therefore, the Pauchard '462 patent does not disclose, suggest or teach a structure or method whereby a semiconductor interface layer is securely fused with a multiplication layer.

Further, the Clark '631 patent discloses grading layer(s) 106 between the multiplication region 103 and the absorption layer 107, and that one or more grading layers may be utilized (Col. 4, lines 54-65). However, in the Clark '631 patent, each of the layers is stacked in the same process sequentially. Therefore, it is respectfully submitted the disclosure of the Clark '631 patent is different from the structure and methods of the present invention.

In this regard, as to the Clark '631 patent, conventionally, an InP layer is directly coupled with an InGaAs layer and the band-gap difference is large between the two layers, and a problem can occur as to a leak current flowing on the avalanche photodiode. However, in the method and apparatus of the present invention, both a device portion provided with the multiplication layer and a device portion provided with the semiconductor interface layer are separately formed before fusing. At this state, both the device portions are exposed in the air, thereby entering impurity into the device portions with the device surfaces oxidized. Thereafter, the device portions are fused, but, in the case where the interface layer is not provided thereon, the problem of a leak current flowing in the avalanche photodiode can occur as described above.

Specifically, in the apparatus and methods of the present invention, with the multiplication layer being formed of silicon and the absorption layer being formed of a compound semiconductor, considering the difference in these materials, respectively, they are therefore not manufactured in the same process, but, rather, in different or separate processes, with the fusing then being applied thereto. As mentioned previously, in contrast, in the case of the Clark '631 patent, each of the layers is stacked in the same process sequentially.

Further, in contrast, the Razeghi '635 patent's disclosure of Sb based heterostructures likewise does not disclose an avalanche photodiode or a method for manufacturing an avalanche photodiode, as respectively recited in Claims 1, 6, 7 and new method Claim 8.

Therefore, it is respectfully submitted that apparatus and methods of the present invention, as respectively recited in Claims 1, 6, 7 and new Claim 8, are distinguishable from and not obvious over the Clark '631 patent, the Pauchard '462 patent and the Razeghi '635 patent. Dependent Claims 2 through 5 and new dependent Claims 9 through 12 are at least allowable for the same reasons that independent Claim 1, from which Claims 2 through 5 respectively depend, and independent Claim 8, from which Claims 9 through 12 respectively depend, are allowable.

Withdrawal of the rejections of Claims 1 through 7 under 35 U.S.C. § 103(a) is respectfully requested.

Reconsideration and allowance of Claims 1 through 7, and consideration and allowance of new Claims 8 through 12, are respectfully requested.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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